

# CERRO ELECTRONIC DESIGN

## USER GUIDE PHOTOARRAY BOARD

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1/18



## Distribution List

Table 1: Distribution List

Company	Name	Position	No. Of copies
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## Document Revision History

Table 2: Document Revision History

Version	Issue Date	Brief description of Change
V1.0	31-11-2017	Primera versión del documento
V1.1	01-12-2017	Se modifica el apartado <b>iErrorl No se encuentra el origen de la r</b> <b>eferencia.</b> , para incluir la referencia de un conversor USB RS232 TTL que permite la comunicación con un PC.
V2 0	27-03-2019	-Doc. Translation into English
V2.U		- Adaptation to V2.0 of the board



#### ÍNDICE DE CONTENIDOS

1	INTF	RODUCTION	6
	1.1	Acronyms	
	1.2	Document property	
2	BOA	ARD DESCRIPTION	8
	2.1	Top side	
	2.2	Bottom side	
	2.2.1	Power Input:	
	2.2.2	2 R\$485 communication port9	
	2.2.3	3 ADC_Trigger Signal	
	2.2.4	4 Connector USB	
	2.2.5	5 Reset	
	2.2.6	6 Led DL3	
	2.2.7	7 Status Leds	
	2.2.8	8 ID Configuration Switches	
	2.2.9	9 Program connector	
3	RS4	85 COMMUNICATION	11
	3.1	Board ID11	
	3.2	Bus termination12	
	3.3	Debug Port13	
	3.4	Dimensions14	
	3.5	Photodiodes Identification14	
4	FW I	UPDATE	15
5	BOC	OTLOADER FIRMWARE RECORDING (PRODUCTION)	17



#### **FIGURES LIST**

Figure 1: Graphical representation on incident light	. 6
Figure 2: Top side of the board	. 8
Figure 3: Bottom side of PhotoArray	. 9
Figure 4: Communication Pinout connector	. 9
Figure 5: USB to RS485 converter	11
Figure 6: Two boards in the same bus, different ID. (Boards version V1.0)	12
Figure 7: R termination on RS485 bus	13
Figure 8: Debug connector	13
Figure 9: Dimensions of PhotoArray board	14
Figure 10: Photodiodes identification by coordinates	14
Figure 11 : Bootloader Host	15
Figure 12: Firmware update throught USB port	16
Figure 13 : Miniprog3 from Cypress	17
Figure 14: bootloader program	18

#### TABLES LIST

Table 1: Distribution List	2
Table 2: Document Revision History	3
Table 3. Status leds	10
Table 4: RS485 Configuration	11
Table 5. ID configuration	12
Table 6: Pinout TTL serial port, Header 3 pins	13



## 1 INTRODUCTION

This document is the user guide of the PhotoArray board: it describes how to power, the connectors, the LEDs, the configuration switches, etc.

PhotoArray consists of an array of photodiodes and all the necessary elements to measure the current of each of them, digitize them and send them through a serial port.

Following picture shows a graphical view of the incident light to the different photodiodes (or pixels ) on the board:



Figure 1: Graphical representation on incident light

PhotoArray is based on a Cypress PSOC system that manages the readings of the photodiodes. After reading and processing the data, they are sent to a master system through serial communication.

#### 1.1 Acronyms

ADC, Analog Digital Converter

BGA, Ball Grid Array

- DAC, Digital Analog Converter
- ICD, Interface Control Document
- GPIO, General Purpose Input Outputs
- NO, Normally Open



NC, Normally Close

PCB, Printed Circuit Board

OC, Open Circuit

PSOC, Programmable System On Chip

RP, Master

SC, Short Circuit

SMD, Surface Mount Device

SMT, Surface Mount Technology

TBD, To Be defined

TBC, To Be Confirmed

#### 1.2 Document property

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## 2 BOARD DESCRIPTION

#### 2.1 Top side



Figure 2: Top side of the board

On the top side of the board we find the array of photodiodes, **matrix of 7 row by 9 columns** and 9mm pitch.

In the same figure it can be seen that the photodiode (0,0), located in the upper left, belongs to row 0 and column 0.



#### 2.2 Bottom side



Figure 3: Bottom side of PhotoArray

## 2.2.1 Power Input:

Range 9-12V, 1A max.

#### 2.2.2 RS485 communication port

It has the following pin-out:



Figure 4: Communication Pinout connector



Signals A and B are the RS485 signals for RS485 communication.

#### 2.2.3 ADC\_Trigger Signal

ADC\_Trigger is a TTL signal that allows to indicate the capture of a current frame of the photodiodes. A level higher than 5V in this signal will damage the board.

ADC\_trigger signal is high level when signal is inactive. The board detects a falling edge on this signal so does no matter the pulse width.

As this signal is connected to all boards at the same time it can trigger a frame adquisition of all boards in the same bus.

The TS1 button allows the simulation of the HW trigger.

#### 2.2.4 Connector USB

Used for firmware upload.

#### 2.2.5 Reset

This bottom lets a manual reset.

#### 2.2.6 Led DL3

On, indicates the presence of power

#### 2.2.7 Status Leds

Following table explain de leds meaning

Table 3. Status leds

Led	Description
DL1	When it is on, it indicates that the card is waiting for new firmware through the serial port. When the card starts, for 2 seconds this led will be on indicating that it can be updated. Once the 2 seconds have elapsed, this LED remains off during normal operation of the card, except when a HW trigger is received and it will light up briefly. It can be disabled by desoldering the R84 resistor.
DL2	Blinking to indicate that the card is in normal state. At start it remains off. It can be disabled by desoldering the R85 resistor
DL3	Indicates the presence of power, exactly 5V, which are produced form the input power It can be disabled by desoldering the R82 resistor

#### 2.2.8 ID Configuration Switches.

Each board on the bus must have a different ID

#### 2.2.9 Program connector.

It is used in production to record the firmware.



## 3 RS485 COMMUNICATION

Communication with the PhotoArray board take place, at the physical level, through an RS-485 serial port with the following features

Table 4: RS485 Configuration

Parameter	Value
Baud Rate	57600
Data Bits	8
Stop Bits	1
Parity	No
Flux control	No
Configuration	Half duplex

For communication with a PC you can use the free software "Realterm" and a USB-RS485 converter such as the reference USB-RS485-WE-1800-BT, Farnell Code: 1740357.



Figure 5: USB to RS485 converter

Up to 16 PhotoArray boards can be connected on the same bus. The address of each board can be configured using microswitch SW1.

#### 3.1 Board ID

ID of each board can be configured with the SW1 microswitch. Next table specify the microswitch position for each address ID.



Table 5. ID configuration

ID	ID0	ID1	ID2	ID3
0	off	off	off	off
1	on	off	off	off
2	off	on	off	off
15	on	on	on	on

With different ID we can put several boards in the same bus as it shown in the following figure:



Figure 6: Two boards in the same bus, different ID. (Boards version V1.0)

## 3.2 Bus termination

It is recommended RS-485 bus have termination resistors at the start and the end. Photoarray Boards allows to add the termination resistor using SW2. In "On" position termination is added.





Figure 7: R termination on RS485 bus

## 3.3 Debug Port

#### For debug purposes

Table 6: Pinout TTL serial port , Header 3 pins

Pin #		
1	TX	Output
2	RX	Input
3	GND	-



#### Figure 8: Debug connector



#### 3.4 Dimensions



Figure 9: Dimensions of PhotoArray board

#### 3.5 Photodiodes Identification

The position of each photodiode will be fixed by two coordinates (X, Y), where X is the indicative of the columns and Y of the rows.

The photodiode (0, 0) will be located at the top left.







## 4 FW UPDATE

To update the firmware, you need the "Bootloader Host", simple program that is inside the PSOC Creator, (IDE used for the development of the PhotoArray application).

You can download from Cypress or just send us an e-mail and we Will send it to you.

On PSOC creator you can find it on [PSOC Creator x.x.] Tools> Bootloader Host.

The following image shows the result after a successful update.

🛓 Bootloader Host — 🗆 🗙
File Actions Help
🖆 🗎 😂 🞯
File: PHOTOARRAY_v1.0.cydsn\CortexM3\ARM_GCC_541\Debug\PHOTOARRAY_v1.0.cyacd
Ports: Filters Active application: No change V Security key 0x 00 00 00 00 00 00 00 00 00 00 00 00 00
Ready



As you can see on the image, the file to be recorded is: PHOTOARRAY\_Vx.x\_cyacd

When the card is turned on or a reset is done, the DL1 LED will remain lit, indicating that the card is waiting for new firmware. When this happens, we have to select the port that appears in Bootloader Host and click on the record button. This can be done during the first two seconds, after this time the firmware that is currently recorded will take control.



Note: for the update, only the USB port of the card is needed to power it.



Figure 12: Firmware update throught USB port



## 5 BOOTLOADER FIRMWARE RECORDING (PRODUCTION)

This operation will only have to be carried out once, when the cards have been manufactured.

For recording, the following material will be necessary:

- Programmer CY8CKIT-002 Kit, Cypress Miniprog3
   Farnell code: 1753960 (see IError! No se encuentra el origen de la referencia.)
- PSOC Programmer recording software, downloadable free from the Cypress page.
- Recording file: bootloader.hex (supplied by Cerro Electronic Design)



Figure 13 : Miniprog3 from Cypress



The following image shows the image of the programming software after having programmed a board:

		~
PSOC Programmer	- 0	^
File View Options Help		
Pot Selection IV Programmer Utilities JTAG		
MiniProg3/1411DD0001B5 Programming Parameters		
File Path:         C:\Users\Joaquin\Proyectos\CP030_PHOTOARRAY\FWV1.0\CP030_PHOTOARRAY\Bootload           <	ler.cydsn\CortexM3\ARM_GCC_541\	Debug\ >
Programmer. MiniProg3/1411DD0001B5		
Programming Mode:  Programming Mode:  Prover Cycle  Prover Detect		
Verification:      On Off <u>Connector</u> O 5p      10p		
Device Family On Off Clock Speed: 1.6 MHz ~		
CYBCSmot P Programmer Characteristics Status		
Protocol: O JTAG  SWD O ISSP 12C Execution Time: 3.6 seconds		
Voltage: 0 5.0 V      3.3 V      2.5 V      1.8 V      Voltage: 2360 mV		
Actions Results		^
Program Finished at 1		
Programming Succeeded		
Doing Checksum		
Doing Protect		
Programming of Flash Succeeded		
Programming of Flash Starting		
Programming of User NVL Succeeded		
Erase Succeeded		
Device set to CY8C546 262144 FLASH bytes		
Device Family set to		
Automatically petected pevice: CISC5468AXI-DF106		
Floglam Requested at		~
	Activar Windows	
For Help, press F1	PASSa Confeguerectión parconnée	ctedr Wi

Figure 14: bootloader program