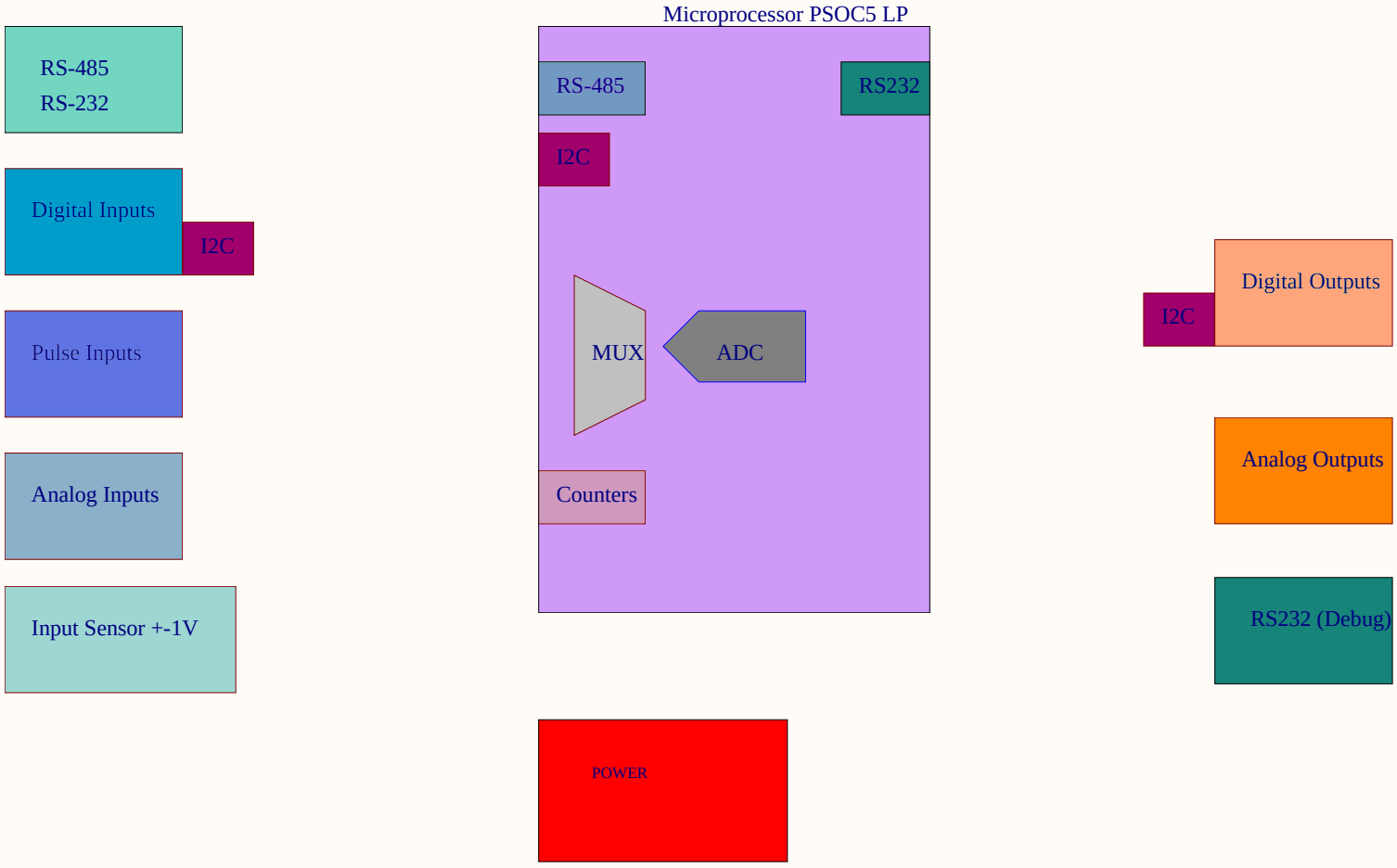
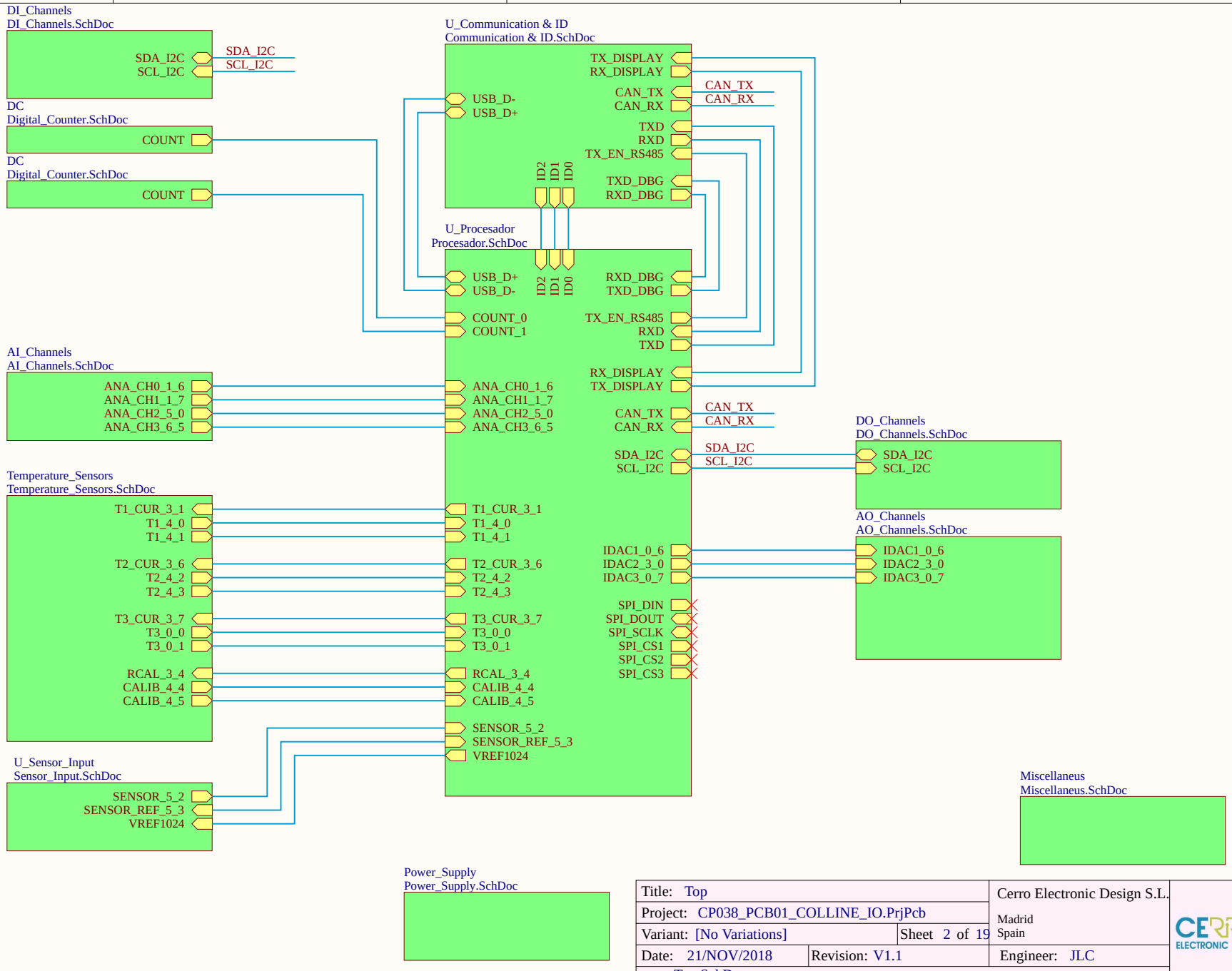


Title: Block Diagram			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]		Sheet 1 of 19	
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Block_Diagram.SchDoc			



Title: Top		Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb		Madrid Spain
Variant: [No Variations]	Sheet 2 of 19	
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC
File: Top.SchDoc		

PROTECTION CIRCUITRY

RS-485 INPUT
RS-232 INPUT

HS18
HSN 3V
BORNA RECTA 3P 5.08
J18

D17 12V
D18 12V
D19 12V
CHASSIS
R70 120R0
RTER
TERMINATION RESITOR CLOSE ON SWITCH

RS485-TRANSCEIVER
MOUNTED FOR RS-485
R69 10R0
R64 10R0
U14
VCC B A GND RO RE DE DI
DS485
+5V
GND
DECOUPLING
C66 100nF 50V

FOR SLAVE CONFIGURATION
ONLY ONE ACTIVE
TX_EN_RS485
RX_485 R1 0R RXD
TX_485 R2 0R TXD
TTL SIGNALS TO PSOC5

RS232
U1
VCC GND V- C1+ C1- C2+ C2- V+
C2 0.33uF 16V
C3 47nF
C4 100nF 50V
C5 0.33uF 16V
C6 0.33uF 16V
MOUNTED FOR RS-232
R37 0R
R38 0R
MAX3232IPW
RS232 TTL
TX_DISPLAY
RX_DISPLAY
TX_232 R3 0R
RX_232 R4 0R

TO DISPLAY ON MASTER CONFIGURATION
HS1
HSN 3V
BORNA RECTA 3P 5.08
J1
TX_DISPLAY_RS232
RX_DISPLAY_RS233
R8 100K0
C44 10nF 50V
CHASSIS-DISPLAY
GND

TO CONTROL EXTERNAL TOUCH SCREEN

TTL DEBUG PORT 3V3 COMPATIBLE
UART-TTL
TXD_DBG
RXD_DBG
J27
TX, OUTPUT
RX, INPUT
CON PH 3V
GND

ID CONFIGURATION & RS485 BUS TERMINATATION
PSOC INT. PULL DOWN
ID0
ID1
ID2
SW8
R63 49R9
RTER

USB FOR FW UPDATE ON THE FIELD
D37 SSB44 4A
VBUS
USB_D-
USB_D+
CN2
CON USB B
D33 TVS 5V
D39 TVS 5V
D40 TVS 5V
R114 100K0
C112 10nF 50V
GND
CHASSIS

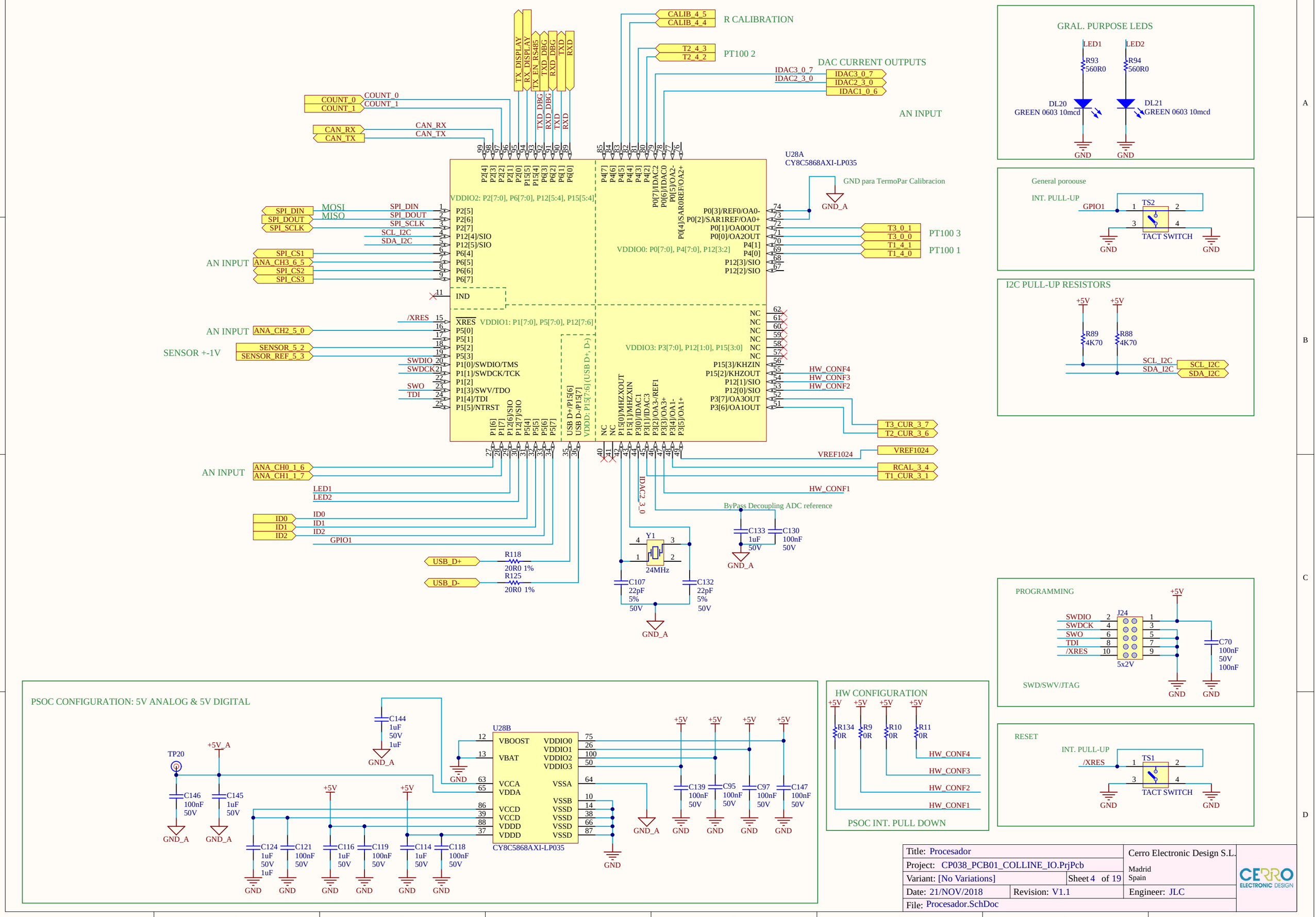
RASPBERRY-PI INPUT
J3
CON PH 20x2V
+3V3_RP1_Out
+5V_RP1
TXD1_3V3
RXD1_3V3
Serial Port 1
TTL 3.3v
MOD1
Modulo RaspBerry PI
RP PI

TTL3V3 TO 5V CONVERTER LEVELS
U2
SN74LVC1T45DCK
RX_RP
U4
SN74LVC1T45
TX_RP
DIR: High A-> B
DIR: Low B -> A
C7 100nF 50V
C12 100nF 50V

CAN COMMUNICATION
TTL 5v
CAN_TX
CAN_RX
U12
SN65HVD1050D
D GND VCC R RS CANH CANL VRef
R5 120R0
SW1
SPST
CAN_H
CAN_L
J4
CHASSIS-DISPLAY
BORNA RECTA 3P 5.08
HS7
HSN 3V
CAN BUS TERMINATION
R28 330K
R29 33k2
C13 100nF 50V
C28 50V 100nF 10%

C15 100nF 50V
C14 100nF 50V
BD14 220R 2A
EF1 100nF
I Max = 700mA
C18 10uF 10V
C20 10nF 50V
C21 50V 100nF

Title: Communication & ID			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]		Sheet 3 of 19	
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Communication & ID.SchDoc			

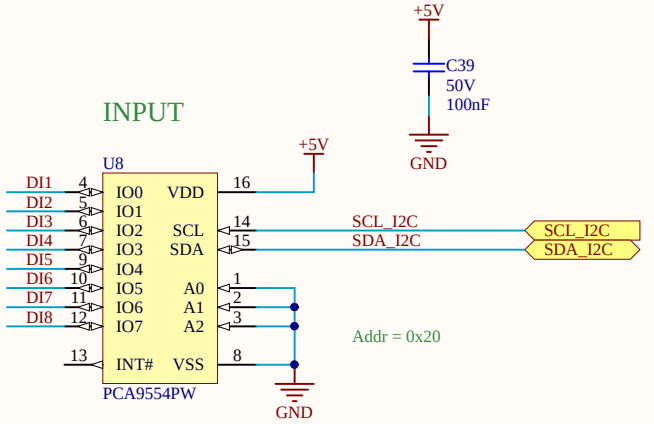


Title: Procesador	Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb	
Variant: [No Variations]	Sheet 4 of 19
Date: 21/NOV/2018	Revision: V1.1
File: Procesador.SchDoc	Engineer: JLC

DI
Digital_Input.SchDoc
DI
DI1
DI
Digital_Input.SchDoc
DI
DI2
DI
Digital_Input.SchDoc
DI
DI3
DI
Digital_Input.SchDoc
DI
DI4
DI
Digital_Input.SchDoc
DI
DI5
DI
Digital_Input.SchDoc
DI
DI6
DI
Digital_Input.SchDoc
DI
DI7
DI
Digital_Input.SchDoc
DI
DI8

DIGITAL INPUT, CHANNELS 1-8

INPUT



FROM PSOC

6.5 Device address

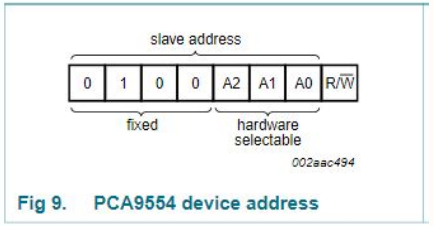
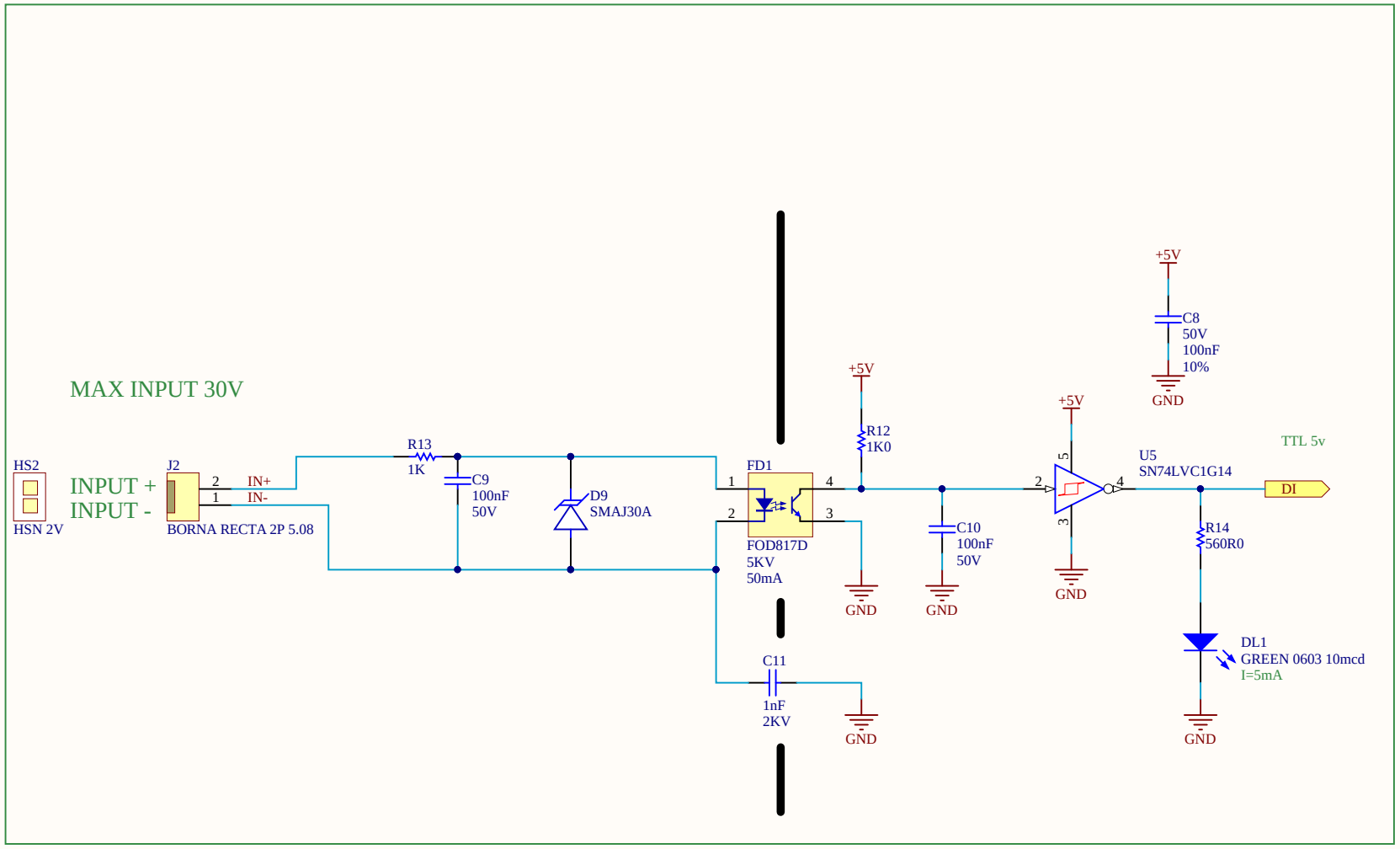
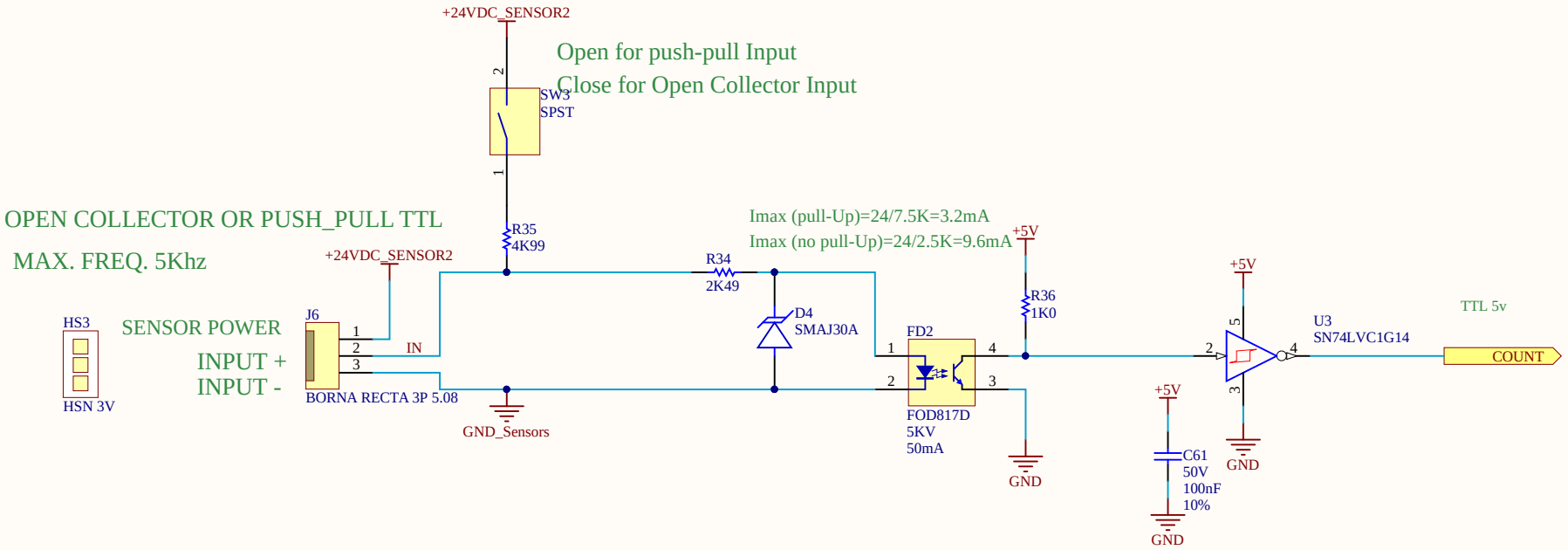


Fig 9. PCA9554 device address

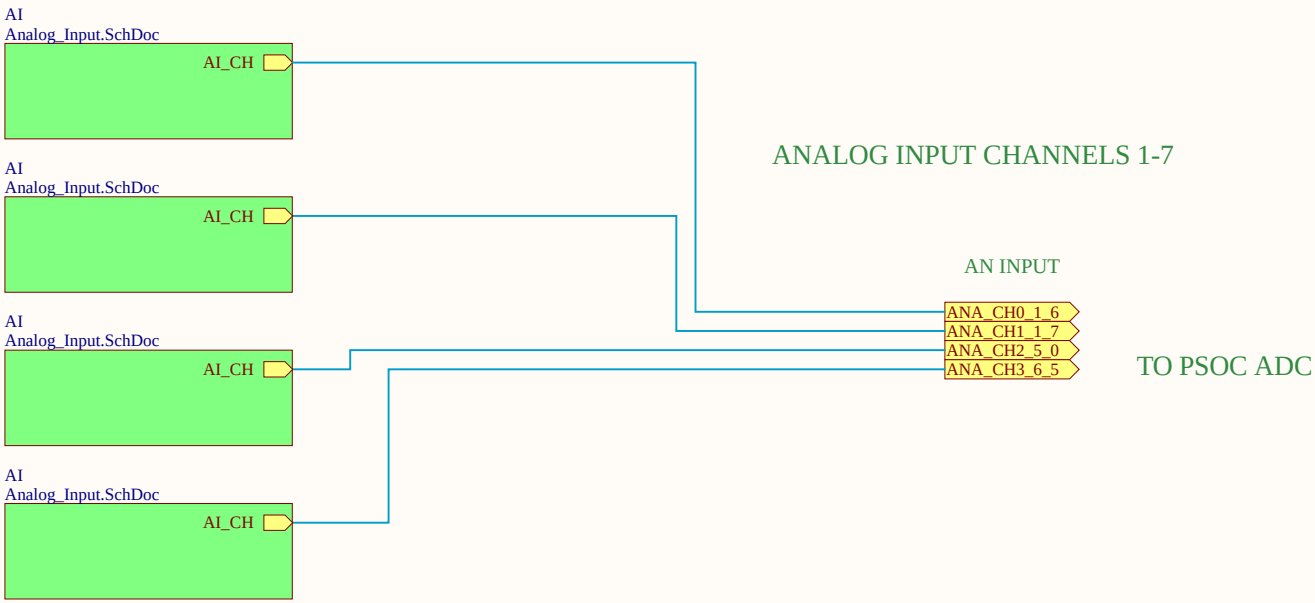
Title: Digital_Input_Channels		Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb		Madrid Spain
Variant: [No Variations]	Sheet 5 of 19	
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC
File: DI_Channels.SchDoc		



Title: Isolated_Digital_Input		Cerro Electronic Design S.L.	
Project: CP038_PCB01_COLLINE_IO.PrjPcb		Madrid Spain	
Variant: [No Variations]	Sheet 6 of 19		
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC	
File: Digital_Input.SchDoc			



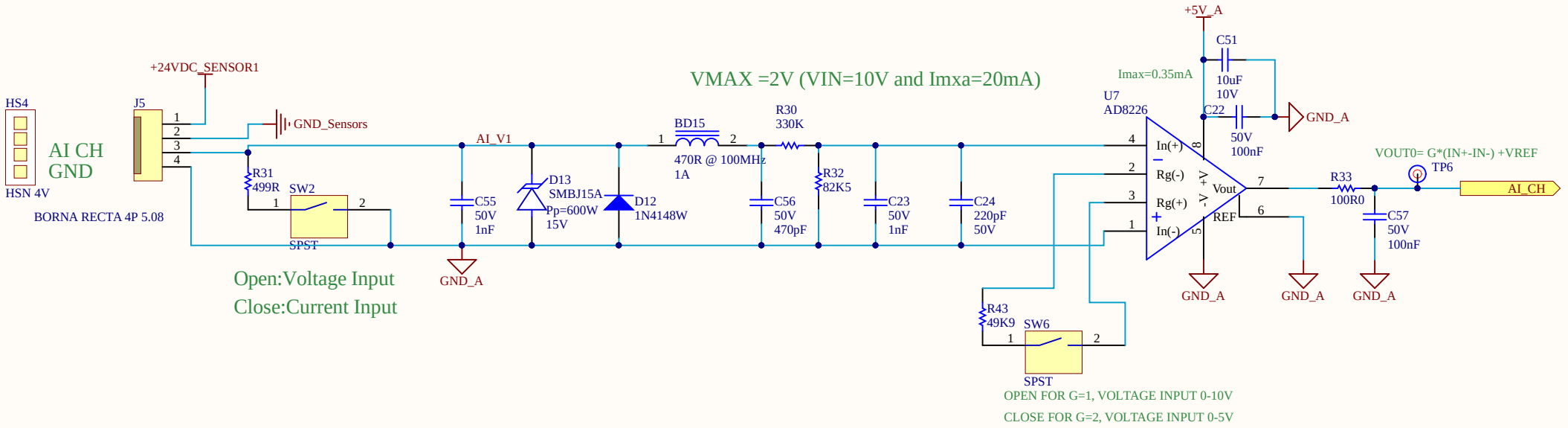
Title: Isolated_Digital_Input			Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb			Madrid Spain
Variant: [No Variations]		Sheet 7 of 19	
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Digital_Counter.SchDoc			

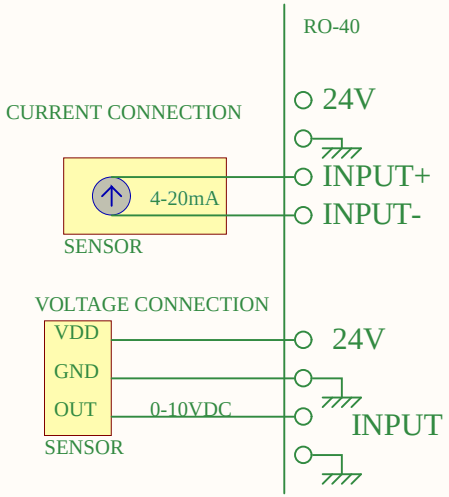


Title: Analog_Input Channels			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 8 of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: AI_Channels.SchDoc			

4 CHANNEL ANALOG INPUT

RANGES: 0-20mA, 4-20mA, 0-5V & 0-10V





Title: Analog_Input_Channels			Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb			Madrid Spain
Variant: [No Variations]	Sheet 9 of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Analog_Input.SchDoc			

DOO
Digital_Output_Optocoupler.SchDoc
Ctrl
DO8

DOO
Digital_Output_Optocoupler.SchDoc
Ctrl
DO7

Optocouplers Output Channels

DO
Digital_Output.SchDoc
Ctrl
DO6

DO
Digital_Output.SchDoc
Ctrl
DO5

DO
Digital_Output.SchDoc
Ctrl
DO4

DO
Digital_Output.SchDoc
Ctrl
DO3

DO
Digital_Output.SchDoc
Ctrl
DO2

DO
Digital_Output.SchDoc
Ctrl
DO1

Standard Output Channels

OUTPUT

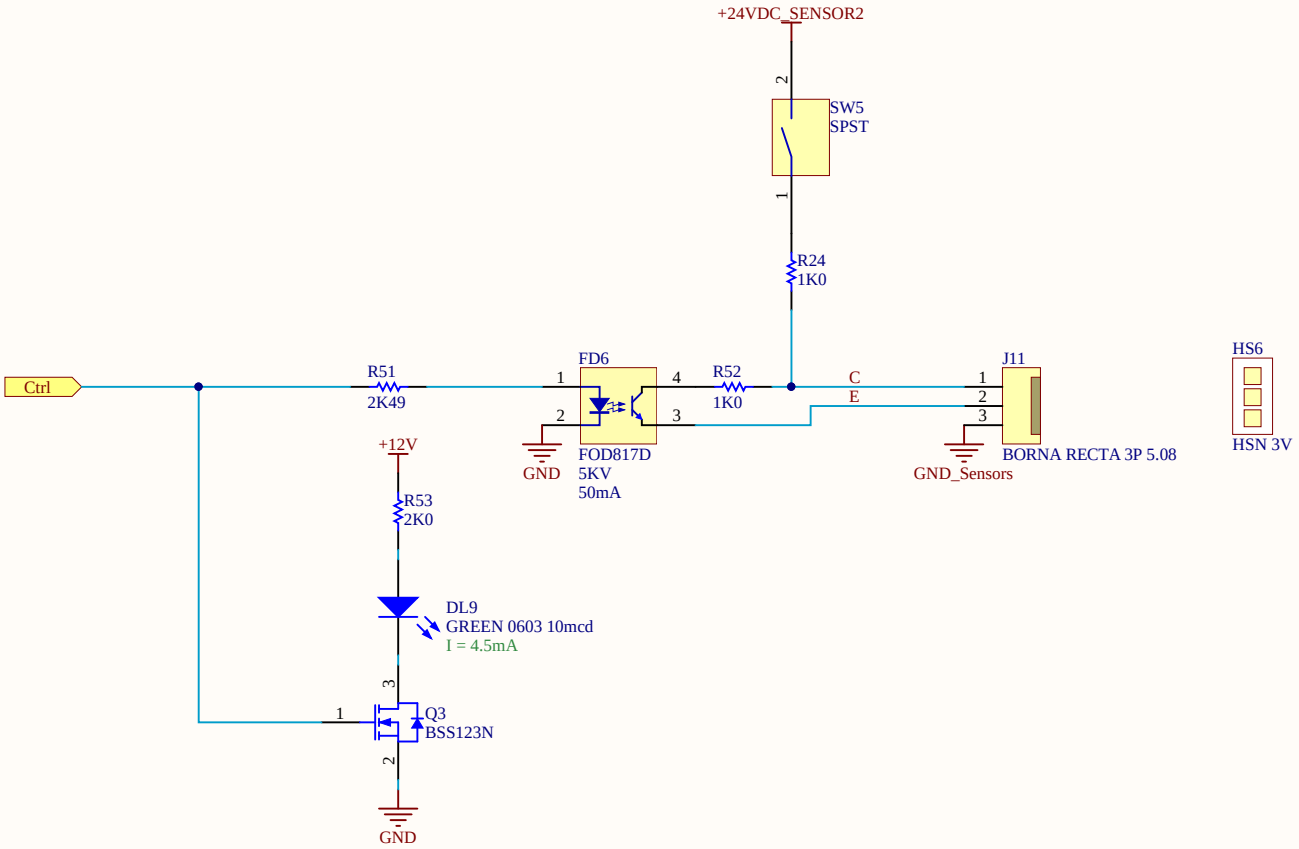
U6
PCA9554PW
IO0 IO1 IO2 IO3 IO4 IO5 IO6 IO7 INT# VDD SCL SDA A0 A1 A2 VSS
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
SCL_I2C
SDA_I2C
Addr = 0x22

R15 10K0
R16 10K0
R17 10K0
R18 10K0
R19 10K0
R20 10K0
R21 10K0
R23 10K0

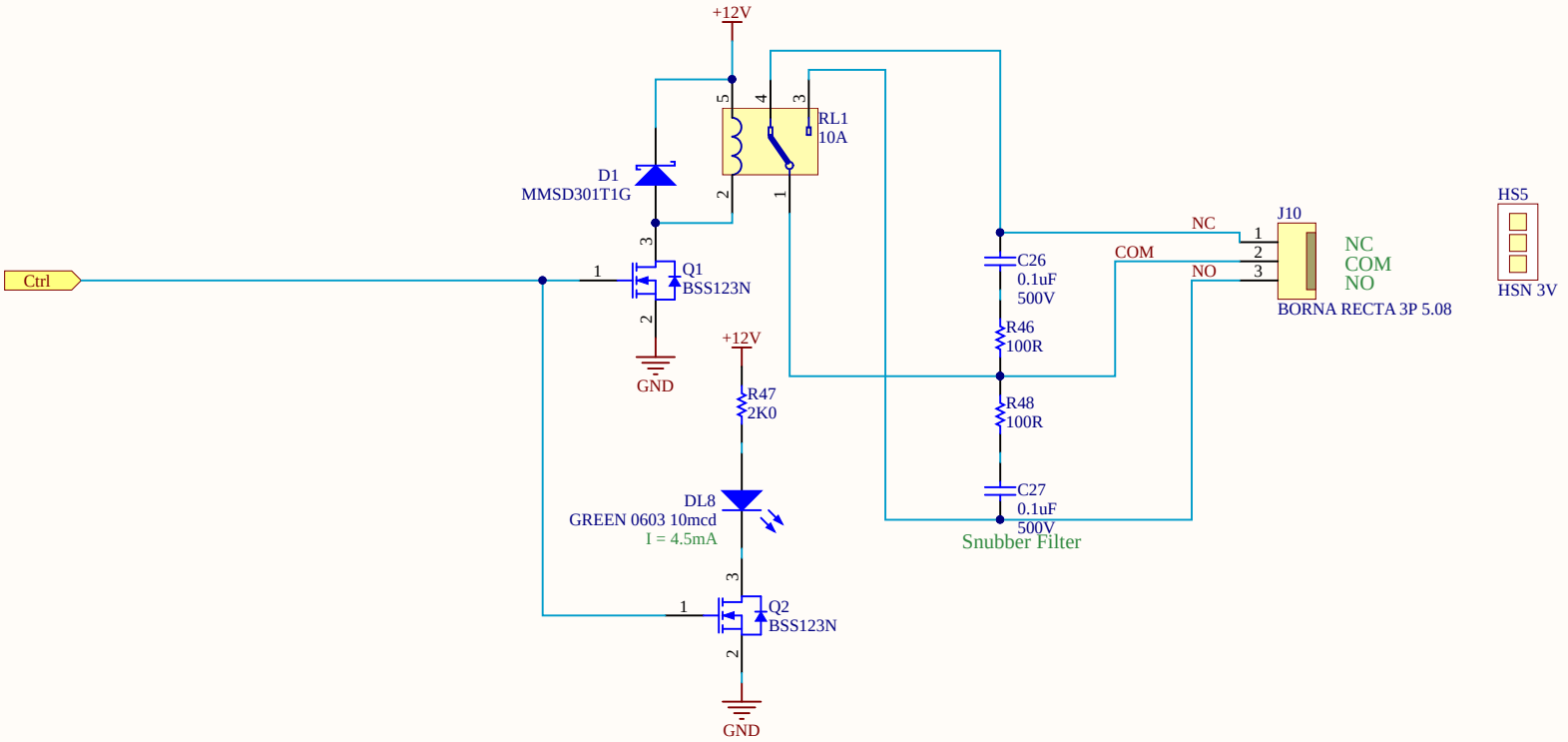
+5V
C30
50V
100nF
GND

FROM PSOC

Title: DO_Channels		Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb		
Variant: [No Variations]	Sheet 10 of 19	
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC
File: DO_Channels.SchDoc		

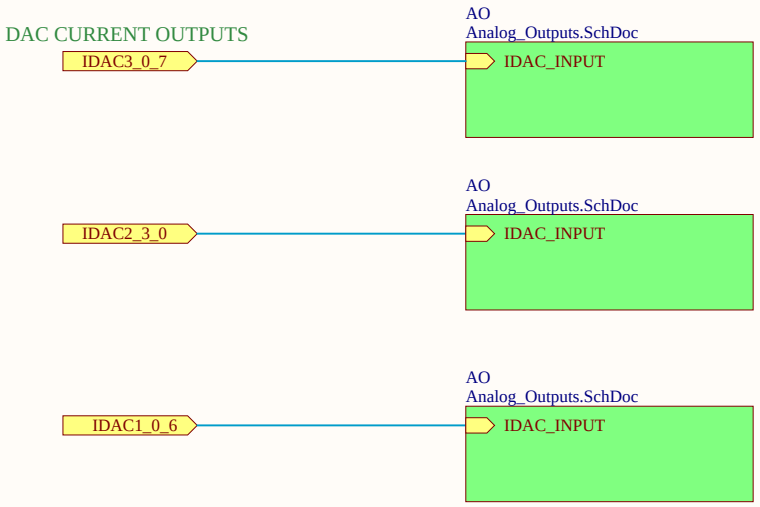


Title: Digital Outputs Optocoupler			Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb			Madrid Spain
Variant: [No Variations]		Sheet 11of 19	
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Digital_Output_Optocoupler.SchDoc			

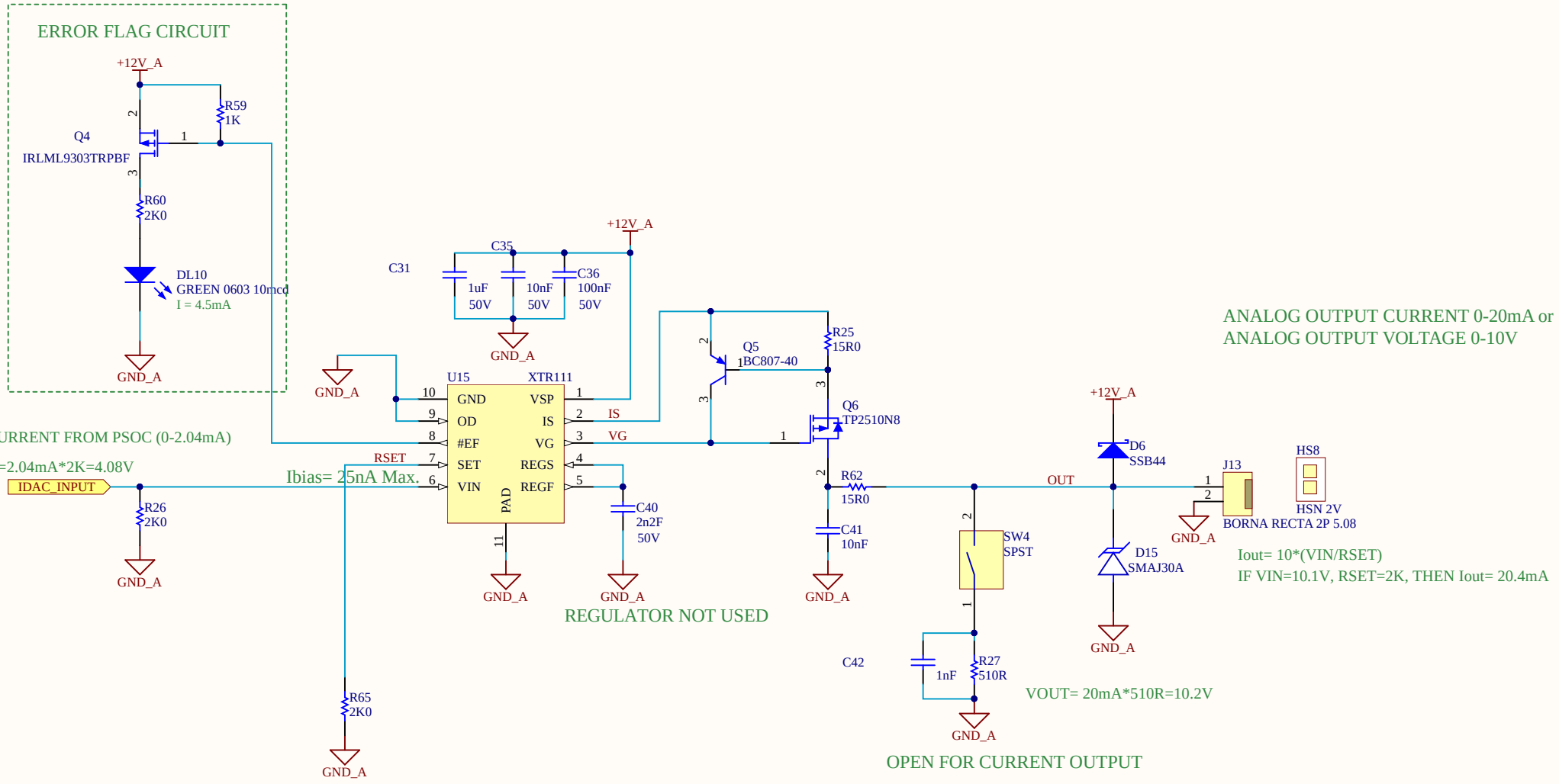


Title: Digital Outputs			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 12of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Digital_Output.SchDoc			

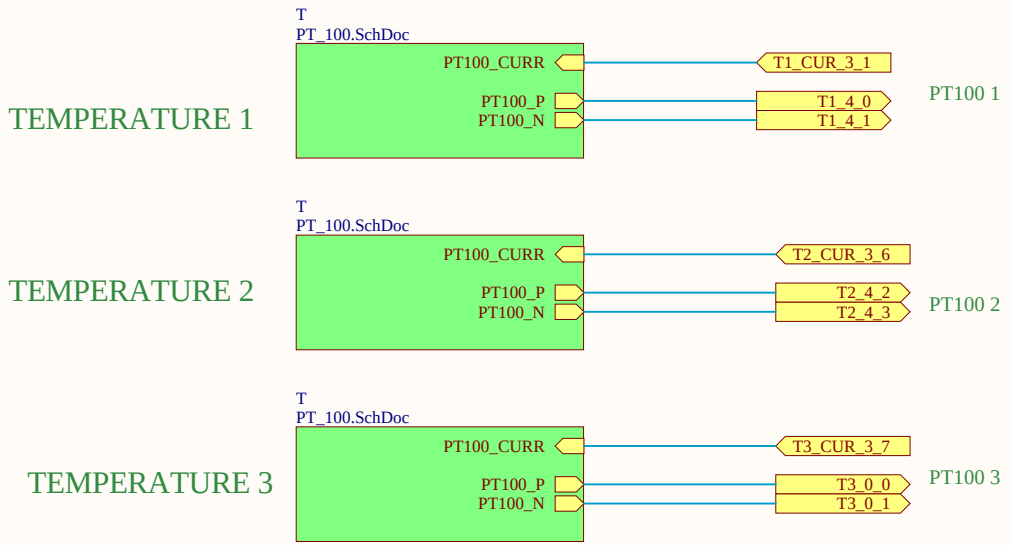
ANALOG OUTPUT, CHANNELS 1-3

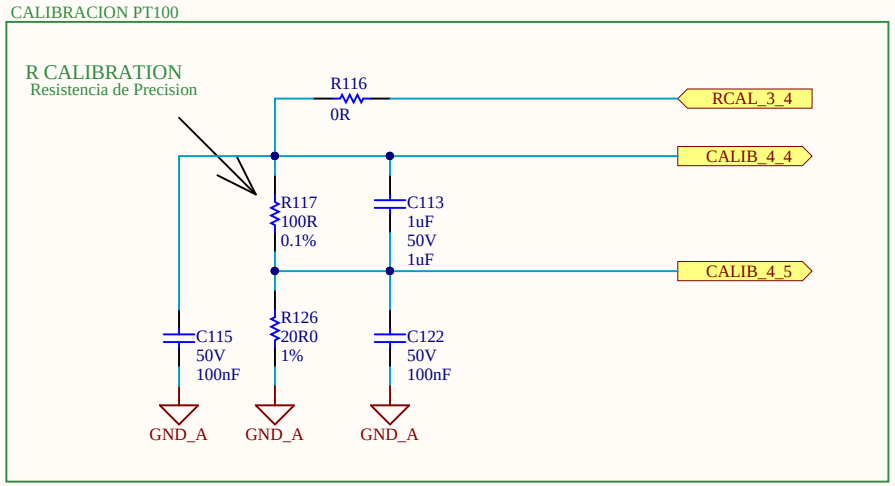


Title: AO_Channels			Cerro Electronic Design S.L.
Project: CP038_PCB01_COLLINE_IO.PrjPcb			Madrid Spain
Variant: [No Variations]	Sheet 13 of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: AO_Channels.SchDoc			

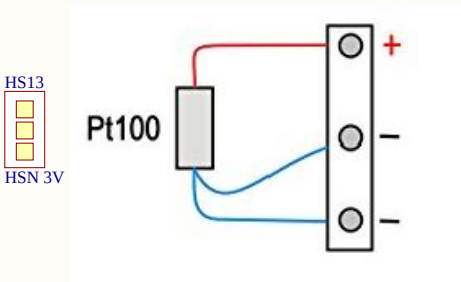


Title: Analog_Ouput			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 14of 19		
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC	
File: Analog_Outputs.SchDoc			





Title: Temperature_Sensors			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 15 of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Temperature_Sensors.SchDoc			



ANALOG POWER

+5V_A

D34
BAV199LT1G
GND_A

PT100_CURR

C90
50V
100nF
D35
SMBJ15A
GND_A

+5V_A
D36
BAV199LT1G
GND_A

PT100_P

J19
BORNA RECTA 3P 5.08
R22
0R
C91
1uF
50V
1uF

PT100_N

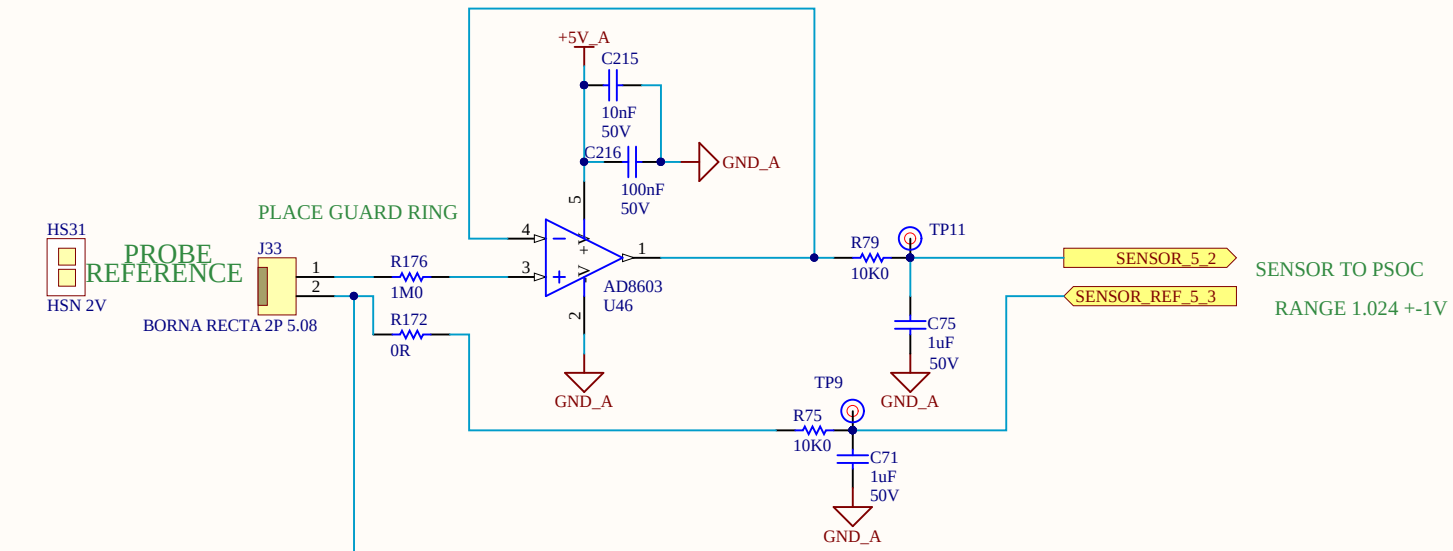
C92
50V
100nF
D2
SMBJ15A
C93
50V
100nF
D38
SMBJ15A
GND_A

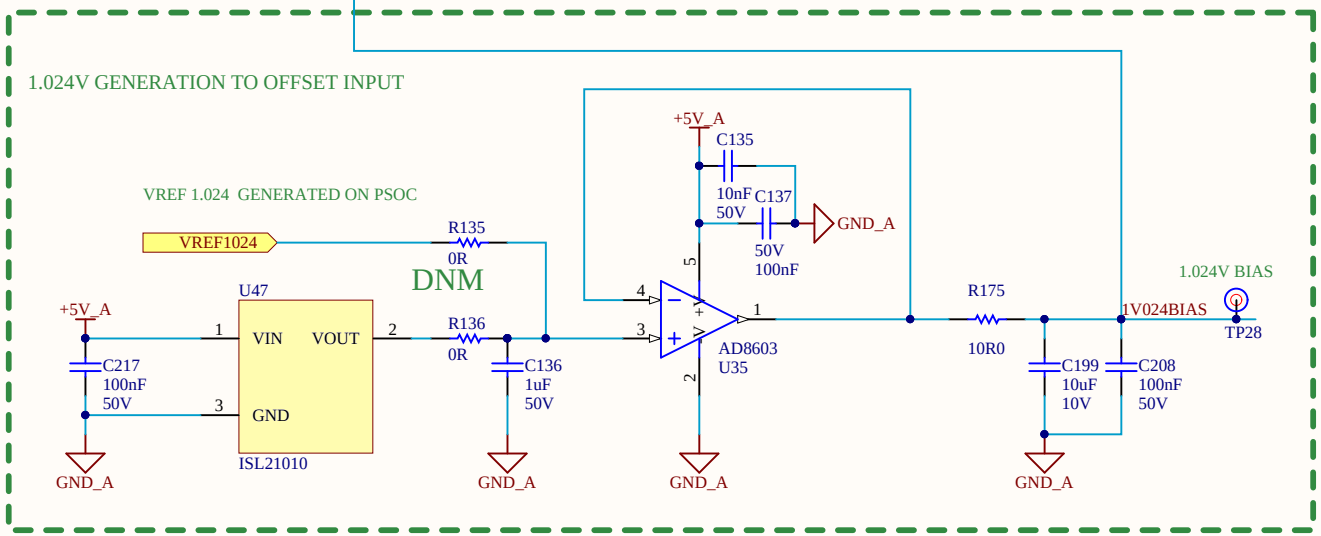
+5V_A
D3
BAV199LT1G
GND_A

C94
50V
100nF
D5
SMBJ15A
R68
20R0
1%
GND_A

Title: PT_100		Cerro Electronic Design S.L.	
Project: CP038_PCB01_COLLINE_IO.PrjPcb		Madrid Spain	
Variant: [No Variations]	Sheet 16of 19		
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC	
File: PT_100.SchDoc			

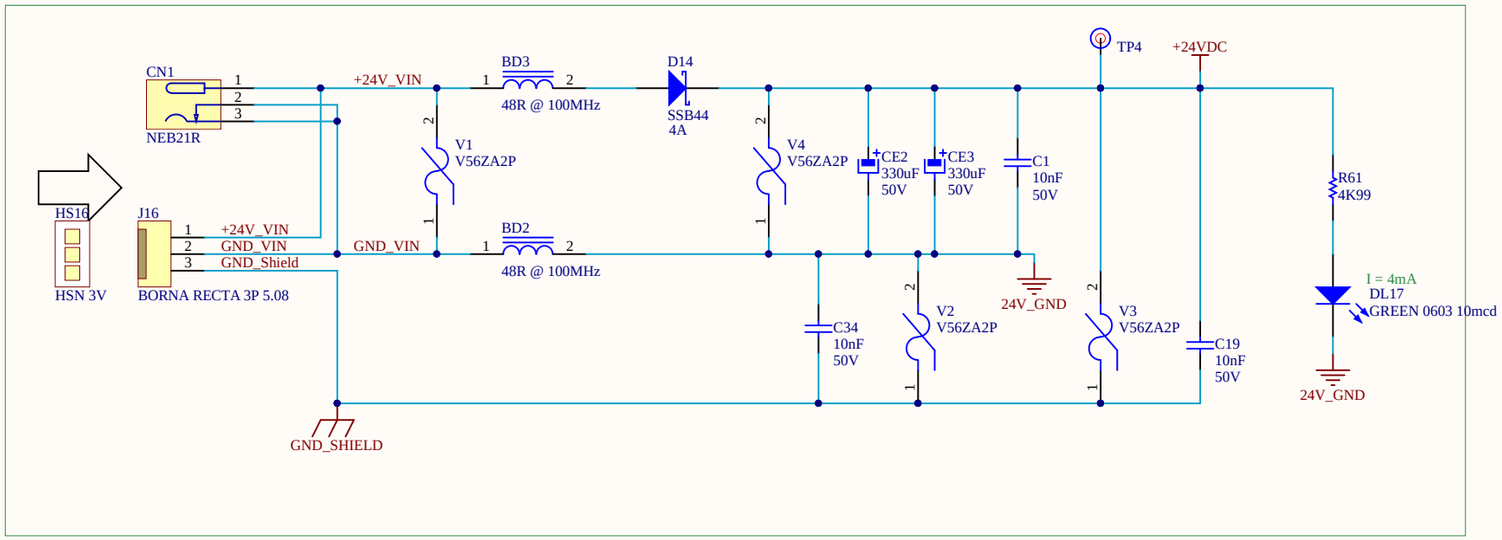
FOR SENSOR WITH OUTPUT +-1V



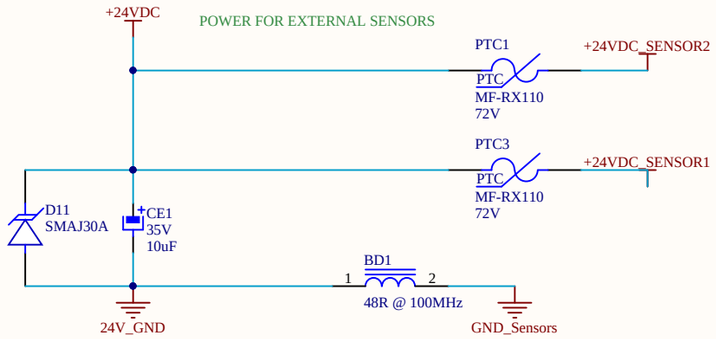


Title: Sensor_Input			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 17of 19		
Date: 21/NOV/2018	Revision: V1.1	Engineer: JLC	
File: Sensor_Input.SchDoc			

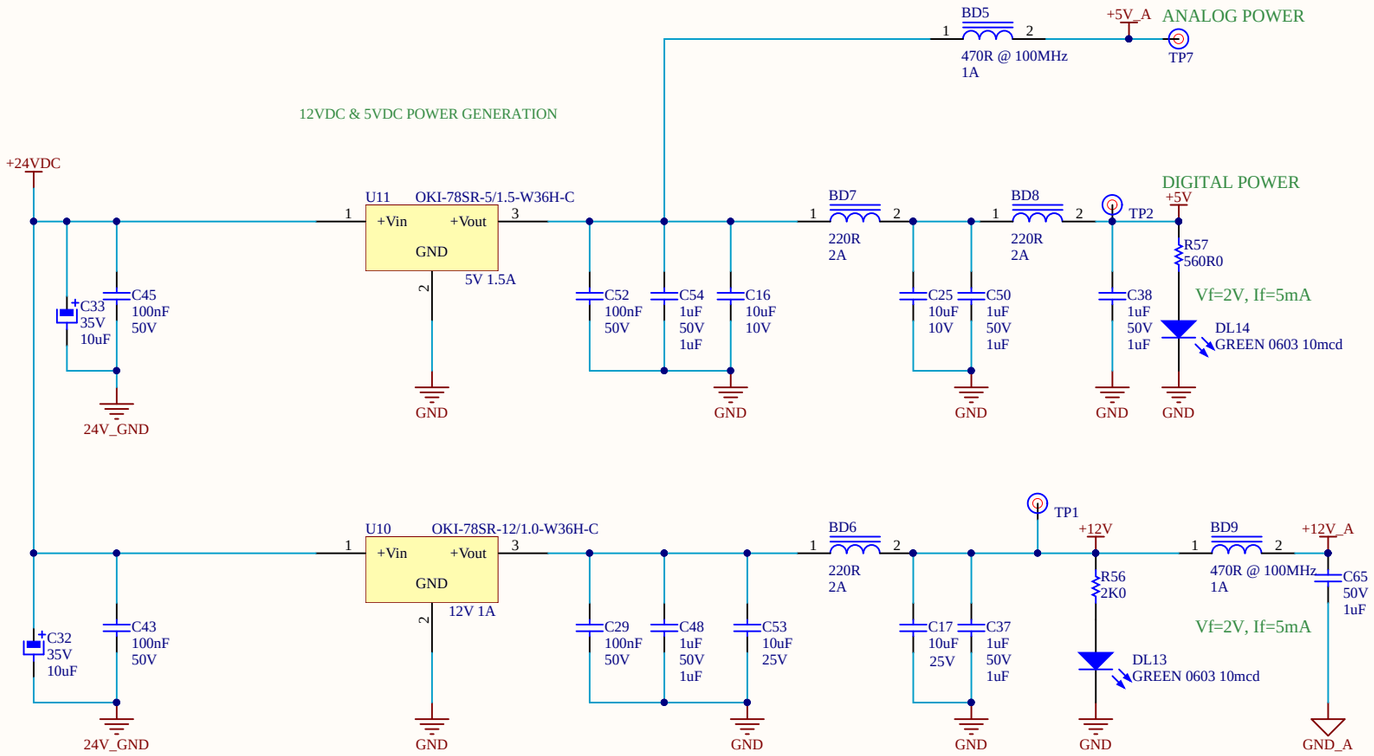
POWER INPUT AND FILTERING

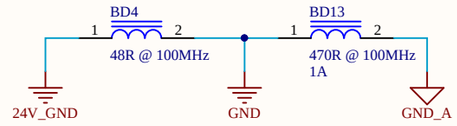


POWER FOR EXTERNAL SENSORS

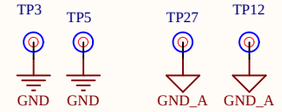


12VDC & 5VDC POWER GENERATION



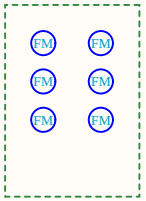


TESP POINT FOR GROUNDS

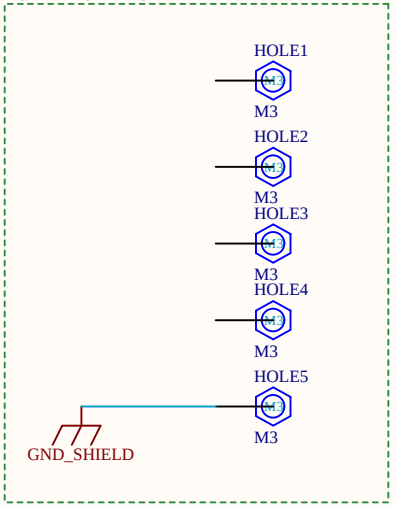


Title: Power Supply			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]		Sheet 18 of 19	
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Power_Supply.SchDoc			

FIDUCIAL MARK



BOARD HOLDERS



PCB

PCB

CP038-PCB01-COLLINEIO-V1_0

Title: Miscellaneus			Cerro Electronic Design S.L. Madrid Spain
Project: CP038_PCB01_COLLINE_IO.PrjPcb			
Variant: [No Variations]	Sheet 19 of 19		
Date: 21/NOV/2018	Revision: V1.1		Engineer: JLC
File: Miscellaneus.SchDoc			